21.3 A 5GHz Duty-Cycle Correcting Clock Distribution Network for the POWER6 Microprocessor

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Increasing clock frequencies and use of lower-loss transmission lines have resulted in wavelengths similar to optimal wire lengths for on-chip clock distribution. The transmission lines are usually neither driven nor terminated with their characteristic impedances, therefore significant reflections occur. By careful design, these reflection effects can be used to create a clock distribution that corrects deviations of duty-cycle as well as reduces sensitivity to PVT variations. They can enhance the effective bandwidth of the clock distribution, reduce the number of buffers needed, and reduce jitter and skew. Conversely, if these reflection effects are not considered, the clock distribution may degrade the chip performance. Alternatives to this simple solution, such as differential distributions, or active or passive duty-cycle correction circuits are complex, and require additional design and test resources.

Consider the case where the duty cycle of the driving buffer is less than 50%. Figure 21.3.1 illustrates the duty-cycle degradation in the case of an unoptimized network. This behavior can be changed by the effects of reflection at the ends of the wires. Clock networks that actually correct duty-cycle errors are designed.

In this work, the pulse transmission through the wires is simulated using PowerSpice. Frequency-dependent transmission-line models of the wires are constructed by Aquaia [1].

As an example, a copper distribution wire is chosen that is 3.0μm wide and 1.2μm thick, with spaces of 1.3μm on both sides between it and the adjacent power or ground. There would be no reflection at the ends of a wire if the source and load impedances were equal to the characteristic impedance of the transmission line. The line impedance is about 50Ω in the examples, and the line is terminated by the input of an FET buffer that is a small capacitive load. To achieve full-swing clock signals, the driving buffer has an impedance of less than the characteristic line impedance. There are reflected waves that travel back and forth along the wire until their amplitudes are reduced by absorption of energy by the terminating resistances and the transmission line losses.

Reflected waves have an important effect on the timing of the rising and falling edges at both ends of the wires. If the duty cycle is exactly 50%, the time between the edges will always be the same, and the effects of reflected waves will be the same on both rising and falling edges. If, however, the duty cycle is not 50%, the timing of the rising and falling edges can be influenced in different ways. The most significant effect is that the arrival of a reflected wave can aid or oppose the buffer output transition and thus change the buffer delay.

In the examples, the velocity of pulses along the line is ~90mm/ns, hence a 4.5mm line has a quarter-wave resonant frequency F_Q of 5GHz. A reflected pulse returns to the buffer output after a delay of 100ps. 5GHz duty-cycle correction takes place for a shorter line length of 2.5mm, when the reflected pulse returns after only 55ps. As shown in Figure 21.3.2 (top), a rising clock edge leads to a rising reflected pulse that pulls the driver output further upwards. At 40% duty cycle, the next falling transition occurs early and overlaps the reflected wave (which is still pulling the driver upwards), and it is delayed. If it arrives late, it is no longer opposed and suffers no delay. A similar effect occurs at the falling transition. A 40% duty cycle becomes 41.3%, and 60% becomes 59.1%, both closer to 50%. A typical clock network consists of many such segments in series, so that significant total duty-cycle correction can result. Figure 21.3.3 shows the change in duty cycle at the end of the line as a function of wire length using the same medium strength buffer for all cases, and shows the optimum at 2.5mm. In a similar way, if the line length is fixed at 2.5mm, correction occurs over a frequency range of approximately 3.6 to 6.1GHz.

Another desired feature of clock distribution networks is insensitivity to PVT variations on the buffers. Using reflection effects it is possible to design buffered transmission-line networks with positive, negative, or zero sensitivity to buffer strength. The optimal wire length for duty-cycle correction is shorter than the quarter-wave resonant length of 4.5mm. In contrast, the optimal wire length for buffer PVT insensitivity is longer than the resonant length (Figure 21.3.3). When designed for small buffer PVT sensitivity the buffer switches before the reflection arrives. When the reflection does arrive, it pulls the buffer output towards $V_{DD}/2$, reducing the buffer delay. The PVT insensitivity can be explained by noting that when the driver is stronger, with lower impedance, this reflected wave is less effective at pulling the buffer output back towards $V_{DD}/2$, and the buffer delay actually increases. This is shown in Fig. 21.3.2 (bottom), where the effect has been exaggerated by using an 8mm line with $1/6^{th}$ of the usual resistance.

In addition to the quarter-wave resonance F_Q, higher-harmonic modes exist at odd multiples of F_Q. There are also resonances where the reflected signal makes an odd number of round trips through the wire in a half-cycle before returning to have a small effect on buffer delay: ($F_Q/3$, $F_Q/5$, . . .). The present wires are too lossy to see the effects of the harmonic frequencies, therefore hypothetical wires, having $1/6^{th}$ the resistive losses of the real wires, are simulated. These potential effects are illustrated in Figure 21.3.4, where a minimum in sensitivity occurs for lengths longer than each resonance length.

A clock distribution design for the POWER6 microprocessor is optimized for frequencies exceeding 5GHz using a compromise between duty-cycle correction and PVT insensitivity; the chip is fabricated in 65nm CMOS. Figure 21.3.5 shows simulated and measured duty-cycle correction of the entire network at 5GHz, with a path length of 19.2mm from the clock source, showing agreement. There is reduced correction at 3 and 4GHz. Figure 21.3.6 shows a histogram of 200 clock edge measurements at two locations on the chip using on-chip measurement circuits [2], showing a final duty cycle of (49.5±0.5)% at 5GHz, without the use of active duty-cycle correction circuits.

In conclusion, for 5GHz clock distributions using 3.0μm-wide 1.2μm-thick copper wiring, reflection effects are significant and can be used to optimize bandwidth, duty-cycle correction and insensitivity to buffer PVT variations.

Acknowledgment:
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References:
[1] M. Elfadel, et al., "AQUAIA: A CAD Tool for On-Chip Interconnect Modeling, Analysis, and Optimization," *Dig. Electr. Perf. Electronic Packaging*, vol. 11, pp. 337-340, Oct., 2002.
[2] P. J. Restle, et al., "Timing Uncertainty Measurements on the Power5 Microprocessor," *ISSCC Dig. Tech. Papers*, pp. 354-355, Feb., 2004.

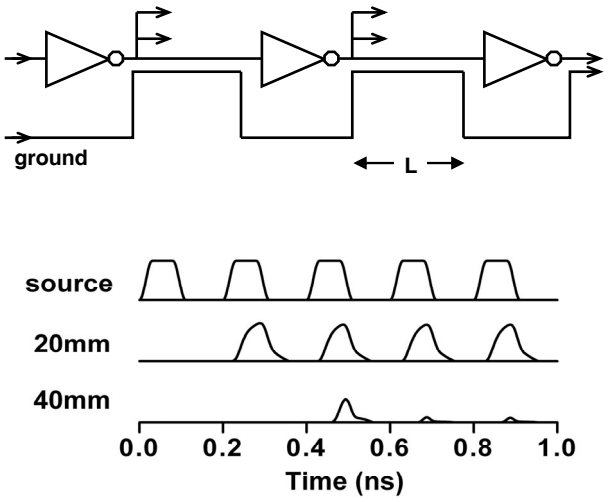

Figure 21.3.1: Waveform degradation as a clock signal is transmitted across a chip using unoptimized wire segments between buffers.

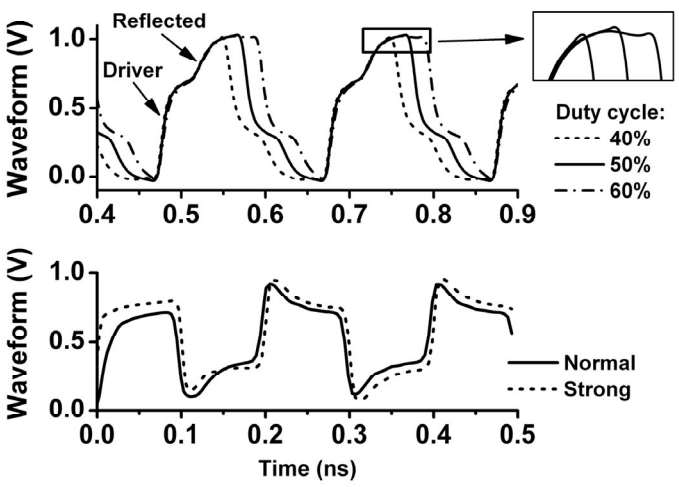

Figure 21.3.2: Top: Buffer output for different duty cycles. Bottom: Output of a nominal and 25% stronger buffer driving an 8mm line.

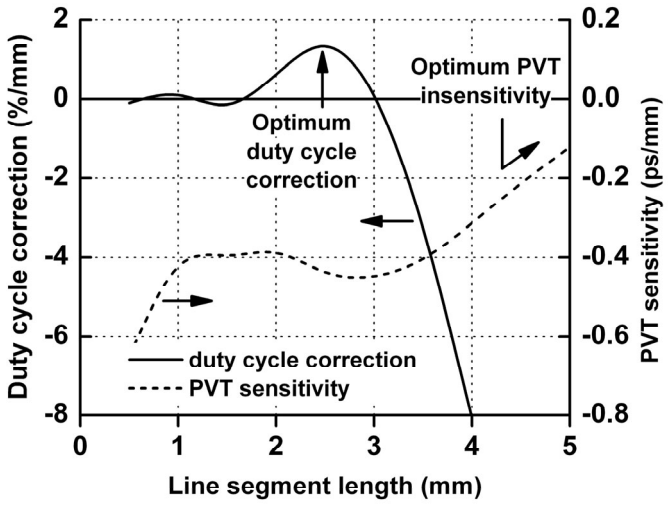

Figure 21.3.3: Duty-cycle correction and the sensitivity of the transit time to small increases in driving buffer strength.

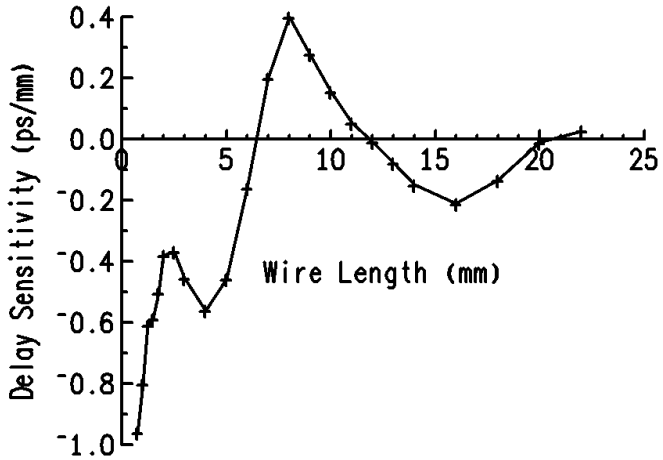

Figure 21.3.4: The delay increase from a 10% increase in buffer drive strength using wires with artificially low resistance.

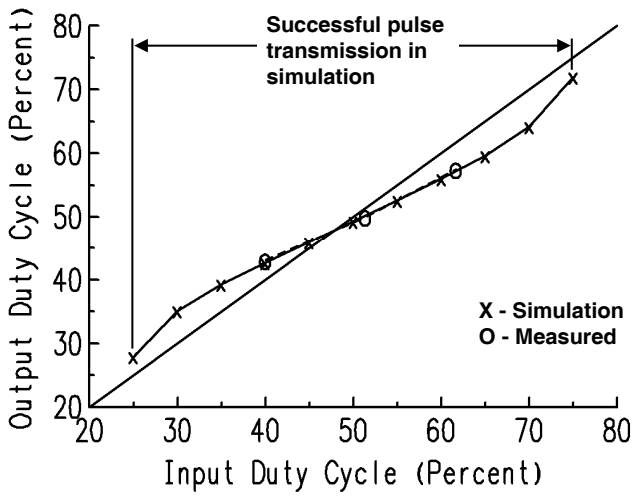

Figure 21.3.5: Simulated and measured duty-cycle correction for an optimized full network at 5GHz.

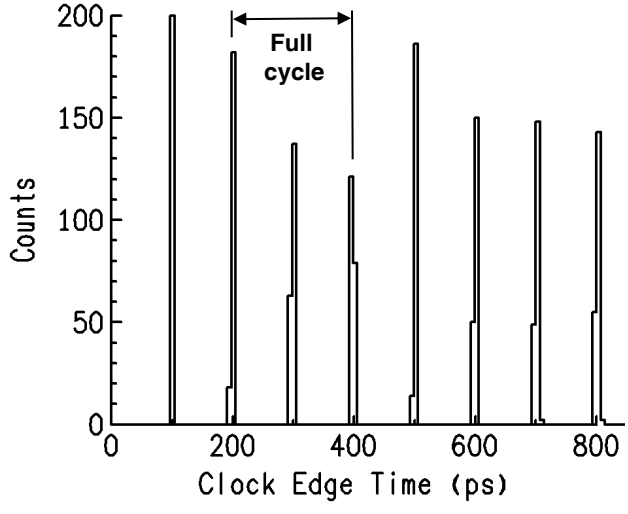

Figure 21.3.6: Clock-edge histogram measured 100 times at each of 2 locations on the chip showing (49.5 ±0.5)% duty cycle at 5GHz.